

## **REMARKS**

Claims 1-12 were examined. All claims were rejected. In response to the above-identified Office Action, Applicant amends claims 1, 2, 5-9 and 12, cancels claims 3 and 4, and adds new claims 13-19. Reconsideration of the rejected claims in light of the aforementioned amendments and the following remarks is requested.

### **I. Support for Amendments**

Claims 1 and 12 are amended to describe more precisely the reset prevention unit. This unit is depicted in Fig. 3 at element 220; the claimed pull-up and pull-down means are shown as transistors MP1, MP2 and MN2. The reset prevention unit and its operation are described in the specification at p. 9, ll. 2-17.

Claim 2 is amended to match the terminology of claim 1 without adding any new matter.

Claims 5-9 are amended to depend from claim 1 instead of (canceled) claim 4, but are otherwise unchanged.

New claims 13-19 recite various features of the power initialization circuit of claim 12. Support for these new claims is at Figure 3 and in the specification at p. 7, l. 17 through p. 9, l. 17.

### **II. Preliminary Discussion**

Applicant asserts that the present invention is definitely different from the cited references, i.e., US 4,902,910 (Hsieh) and US 5,889,416 (Lovett), issued by the Examiner. Applicant wants to traverse Examiner's rejections as follows.

The cited reference does not disclose a first pull-up means and a first pull-down means controlled by a detection signal and a second pull-up means controlled by a delayed detection signal.

In detail, the first and the second pull-up means and the first pull-down means of the present invention do not perform a NAND operation such as a NAND gate of Lovett. Accordingly, the cited references are absolutely different from the present invention. Thus, the claims cannot be rejected by combining Hsieh and Lovett.

### **III. Claims Rejected Under 35 U.S.C. § 112, Second Paragraph**

The Examiner rejected claims 3, 4 and 12 under 35 U.S.C. § 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter applicant regards as the invention. Claims 3 and 4 are canceled in this response, and Applicant has amended claim 12 in a way that eliminates the indefiniteness noted by the Examiner (although not by changing “one” to –another– as the Examiner suggested). Applicant respectfully requests that the rejection of claim 12 on § 112 grounds be withdrawn.

### **IV. Claims Rejected Under 35 U.S.C. § 102(b)**

The Examiner rejected claims 1, 2 and 11 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,902,910 issued to Hsieh (“*Hsieh*”).

Claim 1, as herein amended, recites a power-up circuit comprising a number of elements, including a reset prevention unit where a first pull-up means and a first pull-down means are controlled by a detection signal, and a second pull-up means is controlled by a delayed detection signal. In the Examiner’s analysis, the detection signal and delayed detection signal correspond to nodes 4C’ and 4D’, respectively, of *Hsieh*’s figure 8. However, instead of the claimed pull-up and pull-down means, *Hsieh*’s signals enter NAND gate 83. Of course, a NAND gate may have pull-up and pull-down transistors (as the Examiner discusses later, in connection with a subsequent rejection) but a combination of transistors arranged as required by claim 1 does not implement a NAND logical function.

More specifically, note that transistors MP1, MP2 and MN2 shown in Applicant's Figure 4 are connected as recited by claim 1. The detection signal controls MP2 and MN2, while the delayed detection signal (from delay 20) controls MP1. The truth table of this circuit is shown below (NAND truth table presented alongside for comparison).

MP1/MP2/MN2	0	1
0	1	Z
1	0	0

(Z=high impedance)

NAND	0	1
0	1	1
1	1	0

It is readily apparent that the claimed pull-up and pull-down means operate differently from NAND gate 83 in *Hsieh*. The reference fails to anticipate claim 1 at least because it lacks a structure equivalent to the claimed reset prevention unit. Applicant respectfully requests that the rejection of claim 1 be withdrawn.

Claims 2 and 11 depend from claim 1, and are not anticipated by *Hsieh* for at least the reasons discussed in support of that base claim. Applicant requests that the rejection of these dependent claims be withdrawn also.

#### V. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claims 1-12 under 35 U.S.C. § 103(a) as unpatentable over *Hsieh* (*supra*) in view of U.S. Patent No. 5,889,416 issued to Lovett ("*Lovett*"). The secondary reference is relied upon only for its teaching of a circuit that performs a NAND function. As Applicant notes above, the Examiner is correct that a NAND gate can incorporate pull-up and pull-down transistors. However, the reset prevention unit including pull-up means and pull-down means connected and controlled as recited in claim 1 does not implement a NAND function. Therefore, even assuming that *Hsieh* and *Lovett* properly may be combined, the references fail to teach or suggest at least the claimed reset

prevention unit. Applicant respectfully requests that the rejection of claim 1 as unpatentable over *Hsieh* and *Lovett* be withdrawn.

Claims 2-11 depend from claim 1, and are patentable over the references of record for at least the reasons discussed above.

Claim 12 recites a power initialization circuit comprising several elements, including a reset prevention unit to generate a power-up signal, including pull-up and pull-down means controlled by a detection signal and a delayed detection signal. The reset prevention unit is described identically to the eponymous unit in claim 1, at least as far is relevant to the current rejection, and so the discussion above applies. Since *Hsieh* and *Lovett* lack at least the claimed pull-up and pull-down means, connected and controlled as recited, Applicant respectfully submits that claim 12 is patentable over those references and requests that this rejection be withdrawn.

#### VI. New Claims

Applicant has added claims 13-19 to refine the power initialization circuit of claim 12. These new claims are patentable for at least the reasons discussed in support of their base claim. Consideration and allowance of the new claims is respectfully requested.

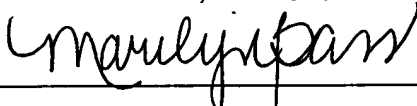


### CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1, 2 and 5-19, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Dated: Feb 8, 2006 Respectfully submitted,  
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<p>12400 Wilshire Boulevard Seventh Floor Los Angeles, California 90025  (310) 207-3800</p>	<p style="text-align: center;"><u><b>CERTIFICATE OF MAILING</b></u></p> <p>I hereby certify that the correspondence is being deposited with the United States Postal Service, with sufficient postage, as first class mail in an envelope addressed to:</p> <p style="text-align: center;">Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450</p> <p> 02-08-06</p> <table border="1" style="width: 100%;"><tr><td style="width: 80%;">Marilyn Bass</td><td style="width: 20%;">Date</td></tr></table>	Marilyn Bass	Date
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